ABSTRACT

A signal delay control circuit for use in a semiconductor memory device is disclosed. The circuit includes a first reference voltage generating unit for generating a first reference voltage; a second reference voltage generating unit for generating a second reference voltage that is lower than the first reference voltage; a control signal generating unit for generating a clock signal to drive input and output operations of internal circuits; and an impedance circuit in circuit with the first and second reference voltage generating units for generating a plurality of reference voltages to be applied to the internal circuits wherein the reference voltages are set in accordance with a distance between the control signal generating unit and the respective one of the internal circuits.

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